Tachysséma EXTENSION MODULES User's Guide

UGEXT_1216 – April 2012

Preliminary Advanced Information

NOTICES

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Safety informations

While unused and packaged, the platform and associated module must be stored in a proper anti static bag.

Proper grounding technique and anti static methods must be carefully used when the module is inserted in the platform and when external connections to the platform are made.

All power supplies must be off when the module is plugged and external connections are made.

Disclaimer

The information contained in this guide is accurate to the best of our knowledge, but may evolve due to corrections or technical progress without notice.

Package content

Your extension package must contain the following items: Extension board(s)

Supporting documents, supporting project files, and technical examples can be downloaded from the Tachysséma web site: www.tachyssema.com

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1 EXTENSION OVERVIEW

1.a Platform Description

The PF101 and PF120 platform kits are accompanying accessories to the LP and HV3 modules. They can be used for rapid prototyping and development, evaluation, and stand alone embedded applications.

These kits include all the necessary circuits to use the LP and HV3 module as well as several interface connectors. Further interfacing capability is offered via extension boards that plug into specific platform expansion slots.

1.b Extension Description

The extension boards plug into one of the two slots available on each platform. Both slots offer power pins as well as a configurable 8 bit bus. In addition, the main slot has dedicated clock and reference pins. Depending on the specific extension requirement, either slot can be used, or one particularly.

The various extension boards available offer the following features and interfaces:

- USB based COM port
- PS2 connector for keyboard interface
- RJ45 connector with Ethernet PHY
- CAN controller
- GPS module with battery back up
- Programmable 7 segment display
- Generic 6/8 bit I/O connector
- User 6/8 position DIP switch
- Prototyping array with 2,54mm pads

The complete schematics for all the extension boards is available for downloading on the Tachysséma web site.

In addition, constraint pin-out files are available for all extension/platform/slot combinations in the form EXT_xx_PFyyy_z.LPF where xx is the extension board number (example 04 for GPS), yyy is the platform type (101 or 120) and z is the slot used (A or B).

2 EXTENSION SPECIFICATION

2.a EXT-01: 7 segment, dip switch, and octal header

This extension offers a 7 segment LED display, an 8 position DIP switch, and an 8 position header for generic IOs. This extension board is compatible with both slot A and slot B. Its two plugs are called HE100 and HE101.

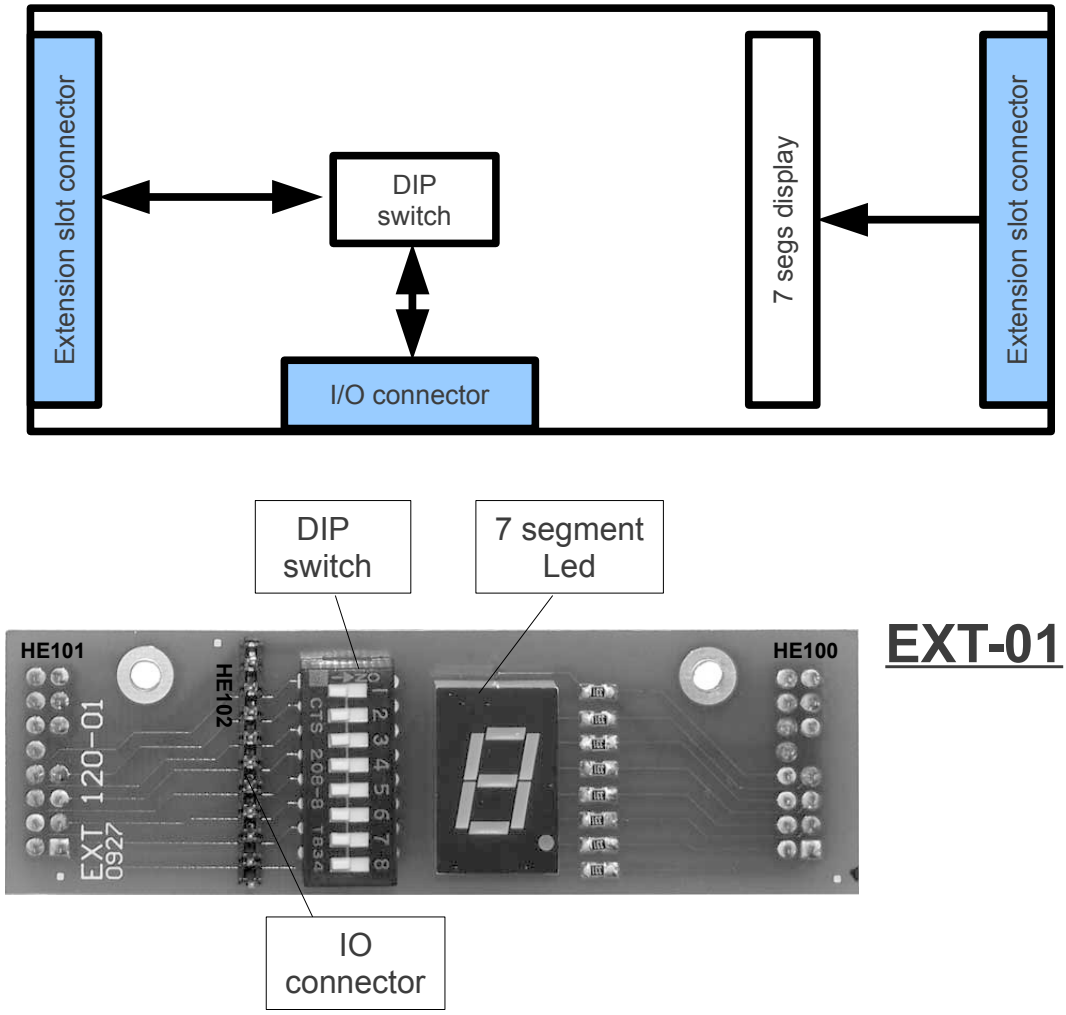


Illustration 1: EXT-01 bloc diagram and picture

When plugged into a PF101 or PF120 platform, HE100 mates into HE4 (slot A) or HE2 (slot B) and HE101 mates into HE3 (slot A) or HE1 (slot B).

Refer to predefined constraint files EXT_01_PF(101/120)_(A/B).LPF when generating an FPGA bitstream.

2.a.1 7 segment Display

This is a standard common anode LED display for user. There are 330Ω current limiting inline resistors for each segment.

2.a.2 I/O connector

This is a 10 pin single row 2.54mm pitch connector. It includes 3.3V power, ground, and 8 bits of generic IOs. Refer to the picture above. This connector is called HE102.

2.a.3 DIP switch

This is a standard 8 bit switch to ground. There are no external pullup resistors. Those internal to the FPGA must be used to read a “logic high”.

2.a.4 Header pinout

Header signal	Function	Alternate function
HE100-1	LED-E	
HE100-2	LED-D	
HE100-3	LED-DP	
HE100-4	LED-C	
HE100-5	LED-G	
HE100-6	LED-F	
HE100-7	LED-B	
HE100-8	LED-A	
HE100-9	KEY	
HE100-10	LED-PWR	
HE101-1	SW8	HE102-10
HE101-2	SW7	HE102-9
HE101-3	SW6	HE102-8
HE101-4	SW5	HE102-7
HE101-5	SW4	HE102-6
HE101-6	SW3	HE102-5
HE101-7	SW2	HE102-4
HE101-8	SW1	HE102-3
HE101-9	KEY	
HE101-10		HE102-2 -- 3R3
HE101-11	SW-GND	HE102-1 -- GND
HE101-12	SW-GND	

Table 1: EXT-01 pinout

2.b EXT-02: RJ45 ethernet interface

This extension offers an ethernet interface via a phyter and RJ45 connector. It must be plugged in slot A as it uses dedicated clock routing resources. Its two plugs are called HE300 and HE301.

2.b.1 RJ45 Ethernet 10/100 interface

This extension card uses a National Semiconductor DP83848C phyter. The RJ45 modular connector has built-in isolation magnetics.

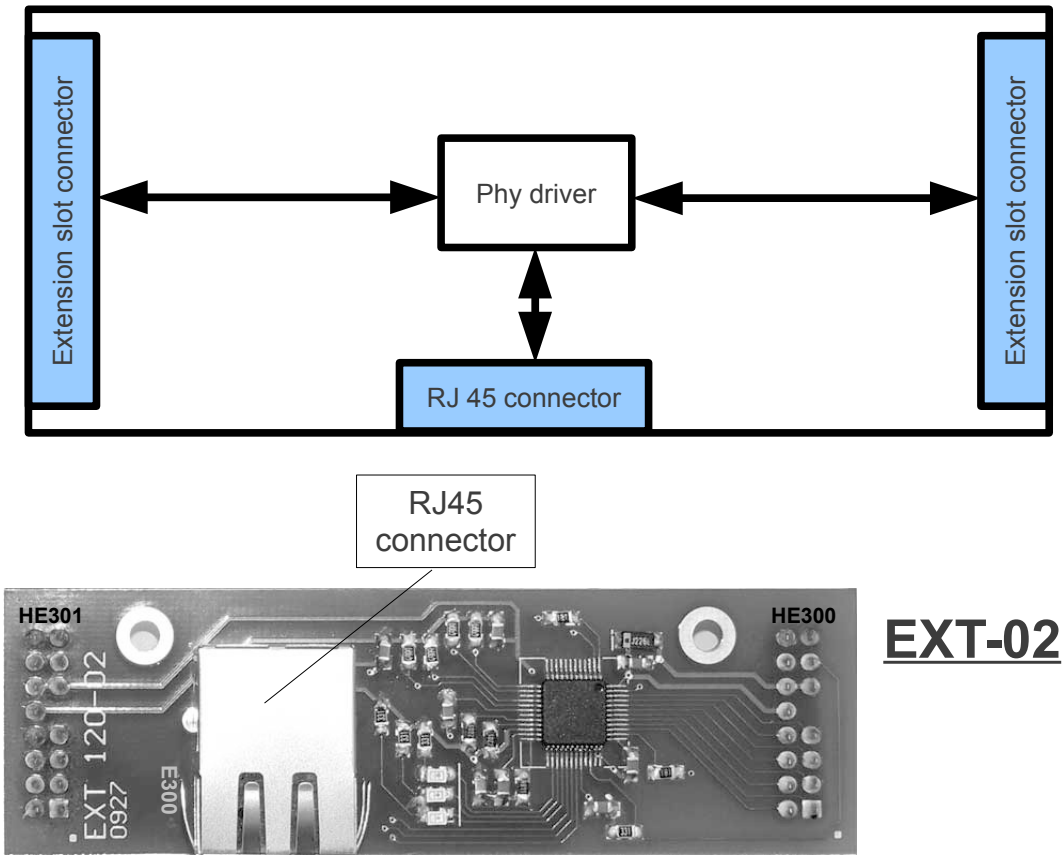


Illustration 2: EXT-02 bloc diagram and picture

When plugged into a PF101 or PF120 platform, HE300 mates into HE4 and HE301 mates into HE3.

Refer to predefined constraint files EXT_02-PF(101/120)_A.LPF when generating an FPGA bitstream.

2.b.2 Header pinout

Header signal	Function
HE300-1	CRS
HE300-2	RX-DV
HE300-3	COL
HE300-4	RX-ER
HE300-5	RX-D1
HE300-6	RX-D0
HE300-7	RX-D3
HE300-8	RX-D2
HE300-9	KEY
HE300-10	PWR-3R3
HE300-11	GND
HE300-12	GND
HE300-13	CLK 25MHz
HE300-16	RX-CLK
HE301-1	MDIO
HE301-2	MDC
HE301-3	TX-D0
HE301-4	RST
HE301-5	TX-D2
HE301-6	TX-D1
HE301-7	INT
HE301-8	TX-D3
HE301-9	KEY
HE301-10	PWR-3R3
HE301-11	GND
HE301-12	GND
HE301-13	TX-EN
HE301-16	TX-CLK

Table 2: EXT-02 pinout

2.c EXT-03: USB serial, keyboard, and CAN interfaces

This extension offers a USB COM port, a PS2 keyboard interface, and a CAN controller with a 5V compatible driver. This extension board is compatible with both slot A and slot B. Its two plugs are called HE200 and HE201.

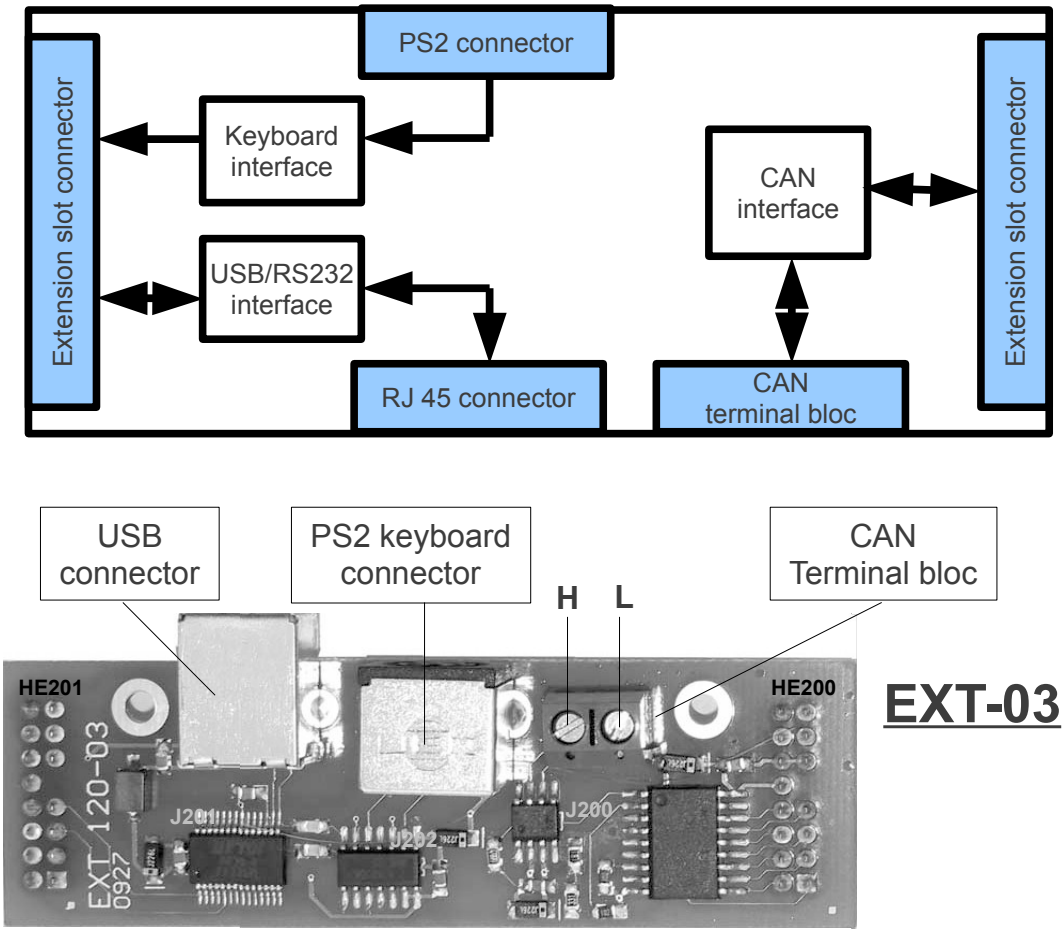


Illustration 3: EXT-03 bloc diagram and picture

When plugged into a PF101 or PF120 platform, HE200 mates into HE4 (slot A) or HE2 (slot B) and HE201 mates into HE3 (slot A) or HE1 (slot B).

Refer to predefined constraint files EXT_03_PF(101/120)_(A/B).LPF when generating an FPGA bitstream.

2.c.1 PS2 keyboard interface

This interface is for a standard PS2 keyboard with a mini DIN-6 connector. It includes a level shifter buffer to make the 5 volt keyboard signals compatible with the FPGA.

2.c.2 USB interface

This USB interface provides a console serial port to a terminal program. The USB B device connector is implemented.

It uses a Future Technology FT232R USB UART circuit.

2.c.3 CAN interface

This CAN interface uses the industry standard Microchip MCP2515 controller and MCP2551 driver.

The physical link is differential copper connected via a terminal block as shown on the picture above.

2.c.4 Header pinout

Header signal	Function	Pinout
HE200-1	CAN-OSC	MCP2515-8
HE200-2	CAN-RX1	MCP2515-10
HE200-3	CAN-RX0	MCP2515-11
HE200-4	CAN-INT	MCP2515-12
HE200-5	CAN-SCK	MCP2515-13
HE200-6	CAN-SI	MCP2515-14
HE200-7	CAN-SO	MCP2515-15
HE200-8	CAN-CS	MCP2515-16
HE200-9	KEY	
HE200-10	PWR-3R3	
HE200-11	GND	
HE200-12	GND	
HE200-14	PWR-P5	
HE201-1	KB-DAT	
HE201-2	CAN-RST	MCP2515-17
HE201-3	KB-CLK	
HE201-5	USB-RX	FT232-5
HE201-7	USB-TX	FT232-1
HE201-9	KEY	
HE201-10	PWR-3R3	
HE201-11	GND	
HE201-12	GND	
HE201-14	PWR-P5	

Table 3: EXT-03 pinout

2.d EXT-04: GPS receiver board

This board is a GPS receiver. It is based around the Vincotech A1035-H module with built-in antenna. This GPS conforms to the NMEA standard. This extension board is compatible with both slot A and slot B. Its two plugs are called HE400 and HE401. Only HE401 is used electrically. HE400 is used as a mechanical support.

2.d.1 A1035-H interface

This extension card uses a Vincotech A1035-H module This module offers a UART based NMEA protocol via the Rx and Tx lines. The 1PPS signal is also available.

A lithium coin battery maintains the GPS last tracking information and real time clock after power is off for faster restart acquisition (TTFF: time to first fix).

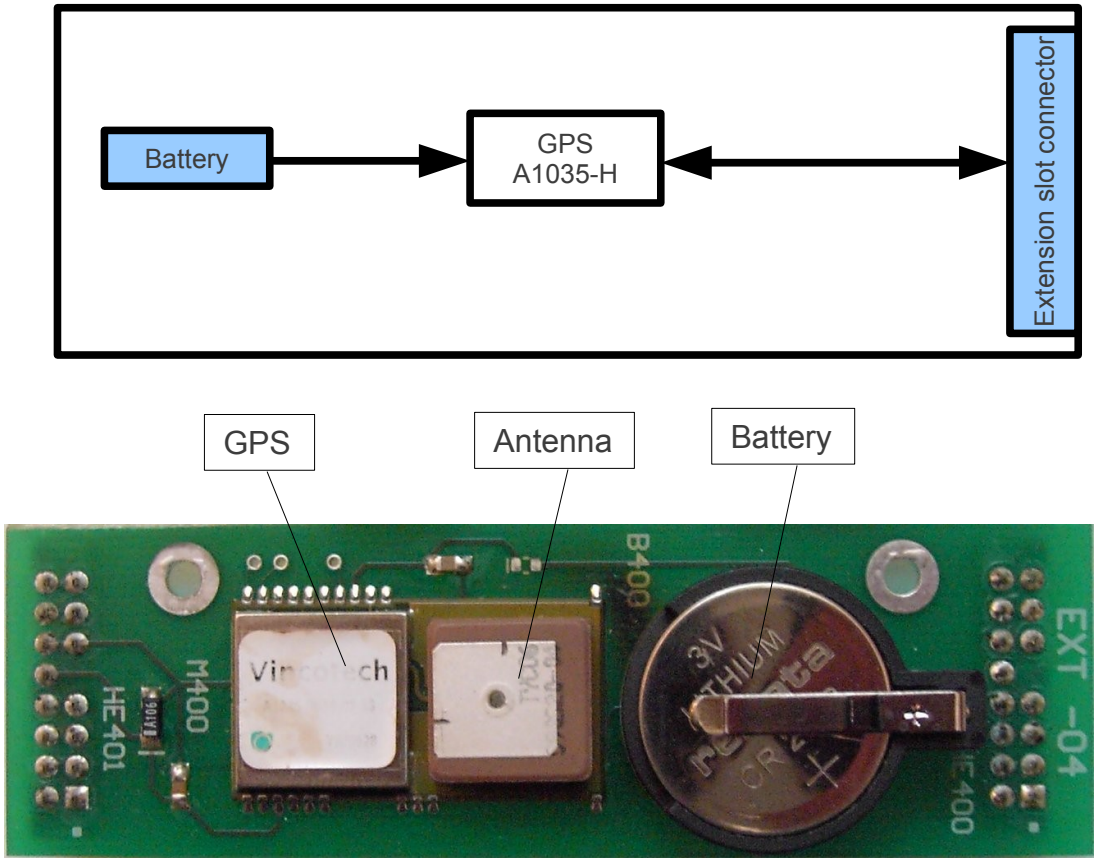


Illustration 4: EXT-04 bloc diagram and picture

When plugged into a PF101 or PF120 platform, HE400 mates into HE4 (slot A) or HE2 (slot B) and HE401 mates into HE3 (slot A) or HE1 (slot B).

Refer to predefined constraint files EXT_04_PF(101/120)_(A/B).LPF when generating an FPGA bitstream.

2.d.2 Header pinout

Header signal	Function	Pinout
HE401-3	GPS-PPS	A1035-H-15
HE401-5	GPS-TX	A1035-H-20
HE401-7	GPS-RX	A1035-H-21
HE401-9	KEY	
HE401-10	PWR-3R3	A1035-H-3
HE401-11	GND	A1035-H-6
HE401-12	GND	A1035-H-6

Table 4: EXT-04 pinout

2.e EXT-05: 7-segment, 6-header/switch, keyboard interface

This extension offers a 7 segment LED display, a 6 position DIP switch, a 6 position header for generic IOs, and a PS2 keyboard interface. This extension board is compatible with both slot A and slot B. Its two plugs are called HE100 and HE101.

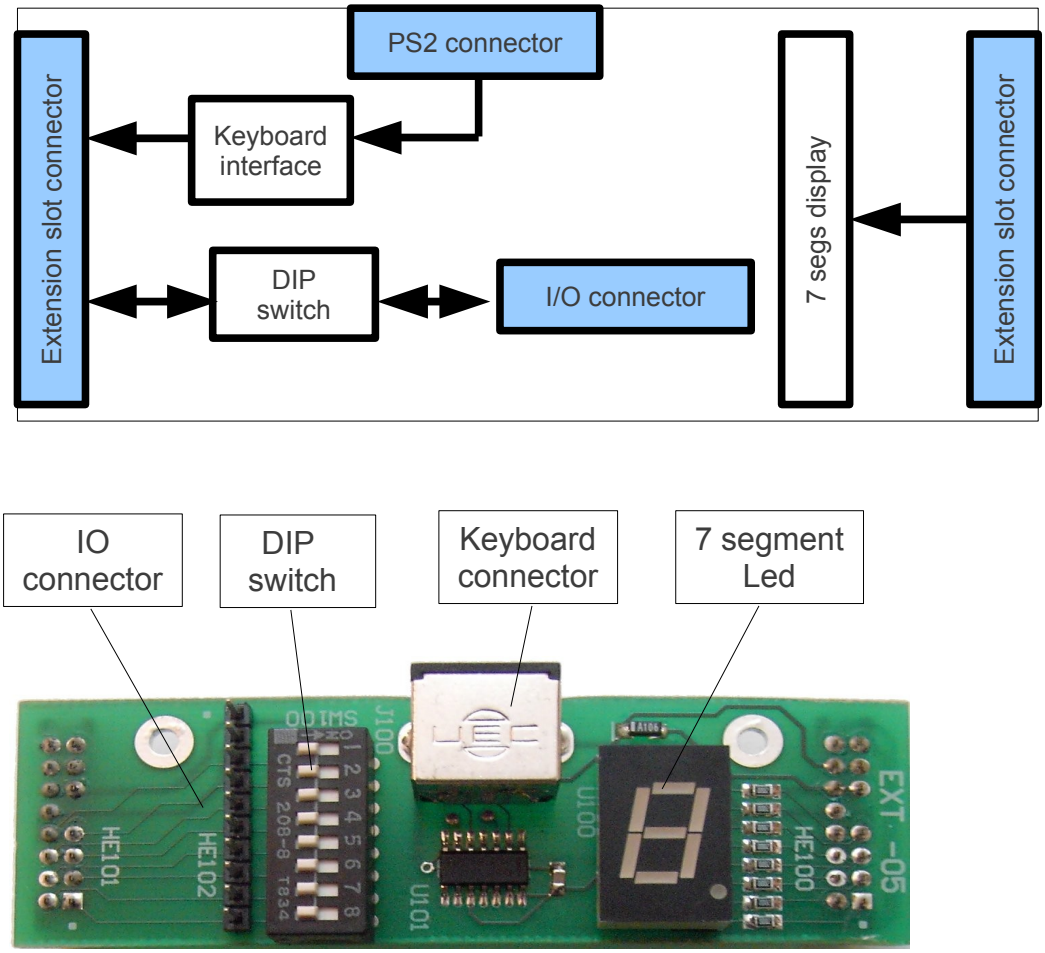


Illustration 5: EXT-05 bloc diagram and picture

When plugged into a PF101 or PF120 platform, HE100 mates into HE4 (slot A) or HE2 (slot B) and HE101 mates into HE3 (slot A) or HE1 (slot B).

Refer to predefined constraint files EXT_05_PF(101/120)_(A/B).LPF when generating an FPGA bitstream.

2.e.1 7 segment Display

This is a standard common anode LED display for user. There are 330Ω current limiting inline resistors for each segment.

2.e.2 I/O connector

This is an 8 pin single row 2.54mm pitch connector. It includes 3.3V power, ground, and 6 bits of generic IOs. Refer to the picture above. This connector is called HE102.

2.e.3 DIP switch

This is a standard 6 bit switch to ground. There are no external pullup resistors. Those internal to the FPGA must be used to read a “logic high”.

2.e.4 PS2 keyboard interface

This interface is for a standard PS2 keyboard with a mini DIN-6 connector. It includes a level shifter buffer to make the 5 volt keyboard signals compatible with the FPGA.

2.e.5 Header pinout

Header signal	Function	Alternate function
HE100-1	LED-E	
HE100-2	LED-D	
HE100-3	LED-DP	
HE100-4	LED-C	
HE100-5	LED-G	
HE100-6	LED-F	
HE100-7	LED-B	
HE100-8	LED-A	
HE100-9	KEY	
HE100-10	LED-PWR	
HE101-1	KB-CLK	
HE101-2	KB-DAT	
HE101-3	SW6	HE102-8
HE101-4	SW5	HE102-7
HE101-5	SW4	HE102-6
HE101-6	SW3	HE102-5
HE101-7	SW2	HE102-4
HE101-8	SW1	HE102-3
HE101-9	KEY	
HE101-10		HE102-2 -- 3R3
HE101-11	SW-GND	HE102-1 -- GND
HE101-12	SW-GND	

Table 5: EXT-05 pinout

2.f EXT-06: Prototyping board

This extension offers the possibility of building a custom interface board. A 190+ hole work area with power distribution is available. All signals from the interface connectors, HE200 and HE201, are brought to the work area.

When plugged in the platform's slot A, both connectors of the board have access to the power supplies, clock, reference, and 8x IO signals. When plugged in slot B, each side has access to the power supplies and 8x IO signals.

The power supplies are 3.3V and 5V, each bypassed on the board with a tantalum capacitor.

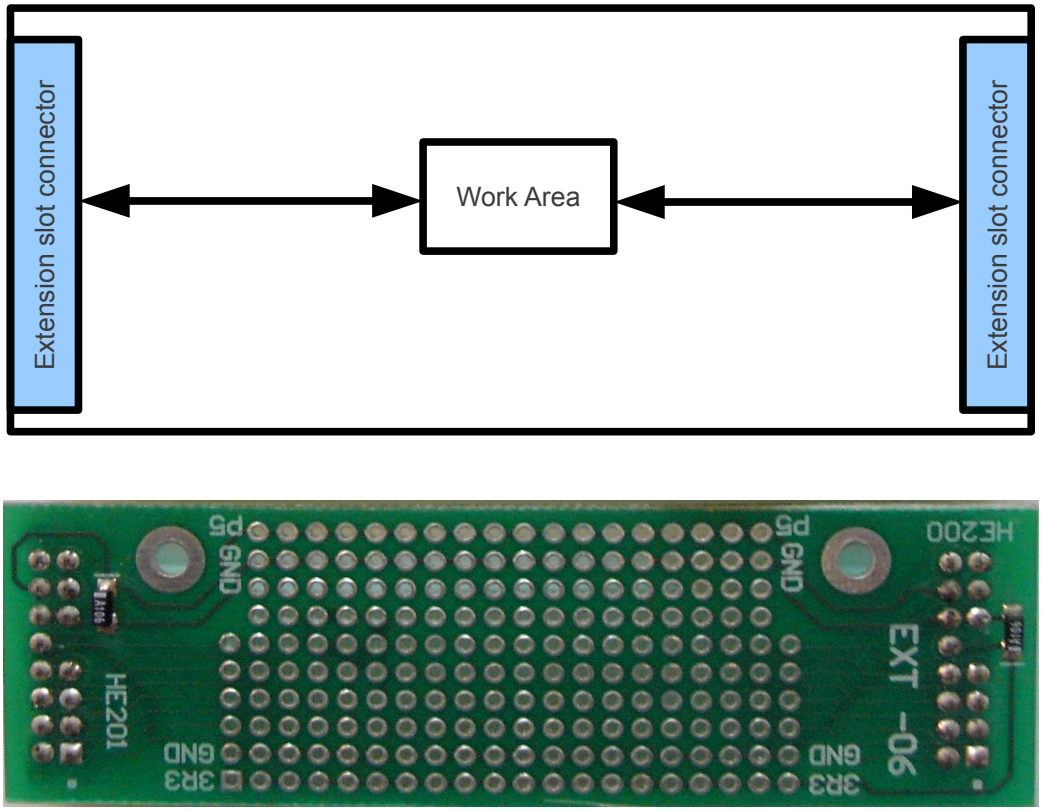


Illustration 6: EXT-06 bloc diagram and picture

When plugged into a PF101 or PF120 platform, HE200 mates into HE4 (slot A) or HE2 (slot B) and HE201 mates into HE3 (slot A) or HE1 (slot B).

Refer to predefined constraint files EXT-06-PF(101/120)-(A/B).LPF when generating an FPGA bitstream.

3 SOFTWARE SUPPORT

Several example projects for these extension boards are available on the platform CDs and for download from the Tachysséma web site. The projects are complete with source code (VHDL and C), predefined configurations, FPGA constraints, and bit streams.

The software support purpose is to guide and help the designer get going fast and easy in using the extension with the platform and module.

4 ADDITIONAL INFORMATION

Tachysséma: More information such as design examples, documentation, applications, technical support, board support packages, development & evaluation boards is available from the Tachysséma web site www.tachyssema.com
Lattice: All Lattice spec sheets and user's guides can be downloaded from the Lattice web site www.latticesemi.com
Future Technology: The USB to RS232 bridge circuit spec sheet and user's guide are available from the Future Technology web site www.ftdichip.com
National Semiconductor: The Ethernet Phyter circuit spec sheet and user's guide are available from the National Semiconductor web site www.national.com
Microchip: The CAN controller and driver circuits spec sheets and user's guides are available from the Microchip web site www.microchip.com